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HiHope RZ/G2 (*) BOARD MB Board

RZ/G2M P/N:R8A774A
RZ/G2N P/N:R8A774B

Rev.4.0

Mounted Note: "NC" means no components

TITLE

 Jiangsu HopeRun Software Co., Ltd	
Title HiHope RZ/G2(*) BOARD MB Board	
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Layout Note:
Following signals need Ground guard.

AUDIO_CLKA
SCIF_CLK, SCIF_CLK_OUT
SD0_CLK_V, SD0_CLK_SOC
SD2_CLK/NFDATA8_V, SD2_CLK_SOC
SD3_CLK/NFWEH_V, SD3_CLK_SOC
AVB_TXCREFCLK
AVB_TXC_25
AVB_RXC_25
QSPI0_SPCLK_18
QSPI1_SPCLK_18
VTHSENSE0_18 until TH1
VTHREF0_18 until TH2

Note: "SD0_WP" and "SD0_CD" signal is fixed at 3.3V.
Note: "SD0_xxx" without "SD0_WP" and "SD0_CD" signal changes to 1.8V and 3.3V by the voltage supplied to the VLD0_SD0.

SDHI0 (CLK,CMD,DAT[3:0])
(1) Matched trace length.

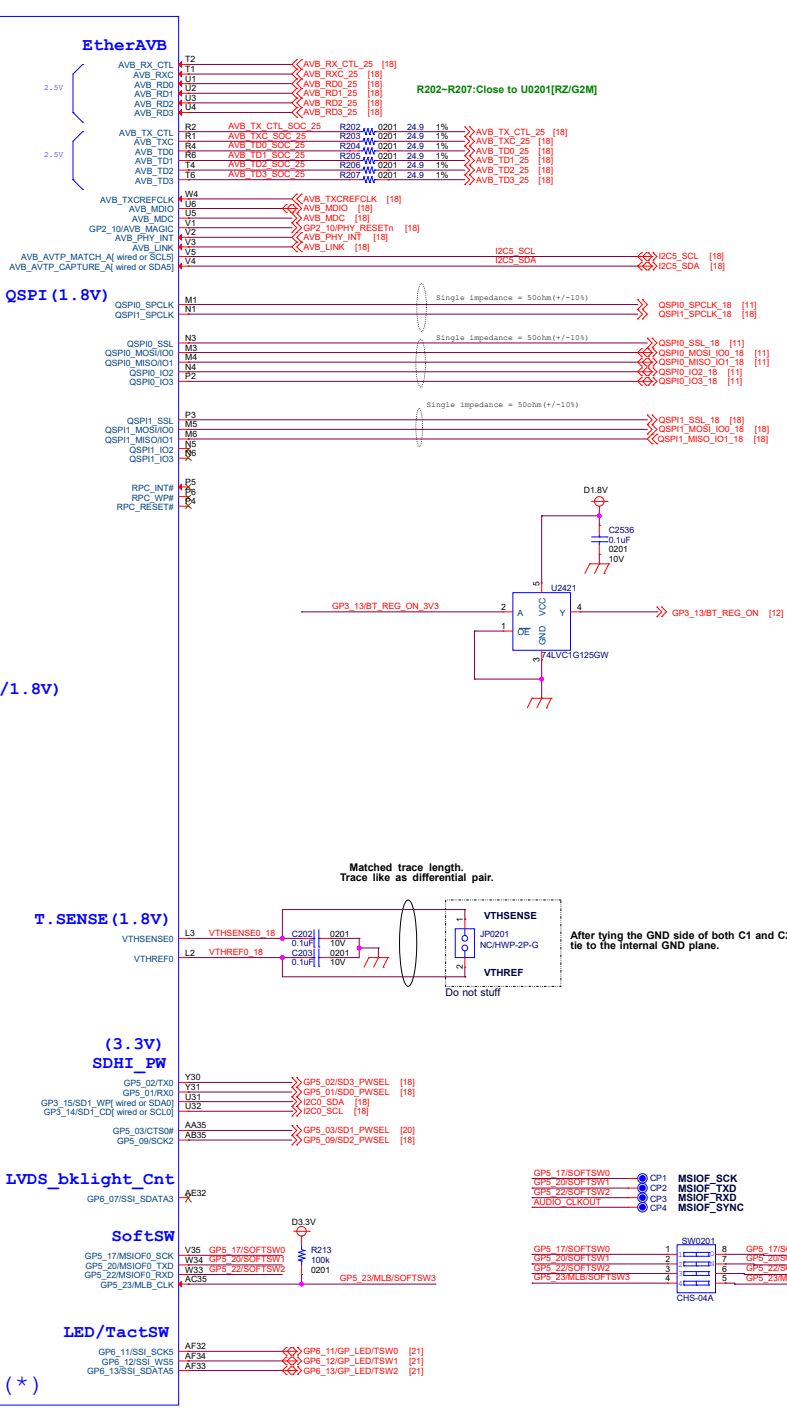
Note: "SD1_xxx" signal changes to 1.8V and 3.3V by the voltage supplied to the VLD0_SD1.
SD1 (CMD,DAT[3:0])
(1) Matched trace length.
SDIO EXT.

Note: "SD2_xxx" signal changes to 1.8V by the voltage supplied to the VLD0_SD2.
SD2 (CLK,CMD,DAT[3:0])
(1) Matched trace length.
WIFIBT

Note: "SD3_xxx" signal changes to 1.8V and 3.3V by the voltage supplied to the VLD0_SD3.
SD3 (CLK,CMD,DAT[7:0])
(1) Matched trace length.
eMMC

Musashi PCB Rev.	GP5_19	GP5_21
3.0	0	0
4.0	0	1
5.0	1	0
6.0	1	1

LPDDR4	GP5_25
K4F6E3S4HM-MGCJ (Samsung 1RANK 16Gbits) x2	0
K4F6E304HB-MGCH (Samsung 2RANK 16Gbits) x2	1



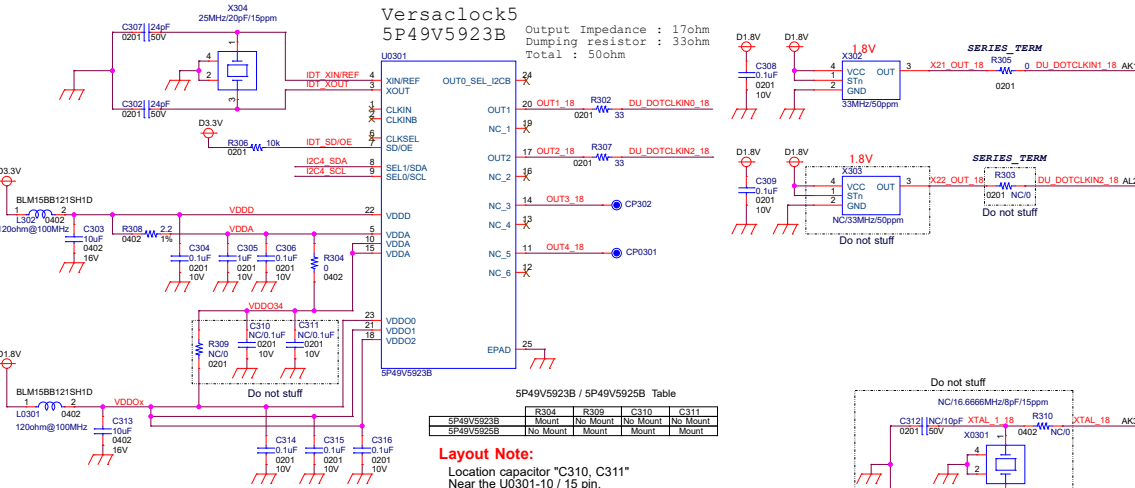
I2Cslave address: 1101_010X

Read:HD5 Write:HD4

VersaLock5
5P49V5923B

Output Impedance : 17ohm
Dumping resistor : 33ohm
Total : 50ohm

CL = 20pF (typ.)



5P49V5923B / 5P49V5925B Table

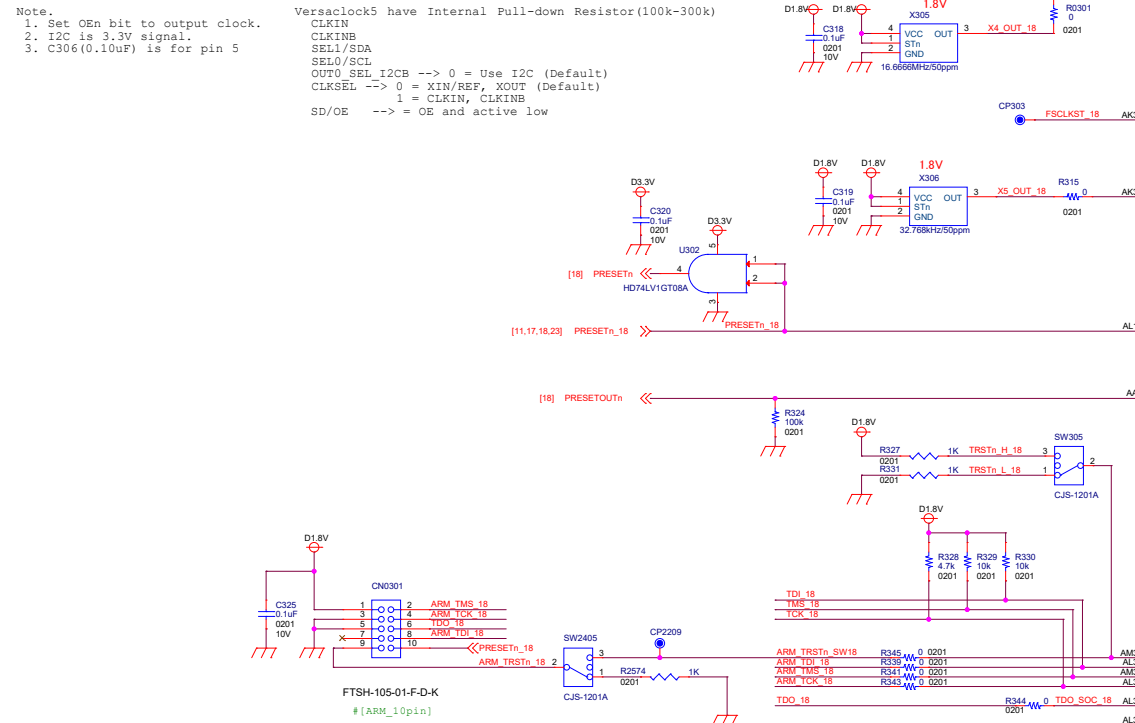
	R304	R309	C310	C311
5P49V5923B	Mount	No Mount	No Mount	No Mount
5P49V5925B	No Mount	Mount	Mount	Mount

Layout Note:
Location capacitor *C310, C311*
Near the U0301-10 / 15 pin.

- Note.
1. Set OE pin bit to output clock.
 2. I2C is 3.3V signal.
 3. C306(0.10uF) is for pin 5

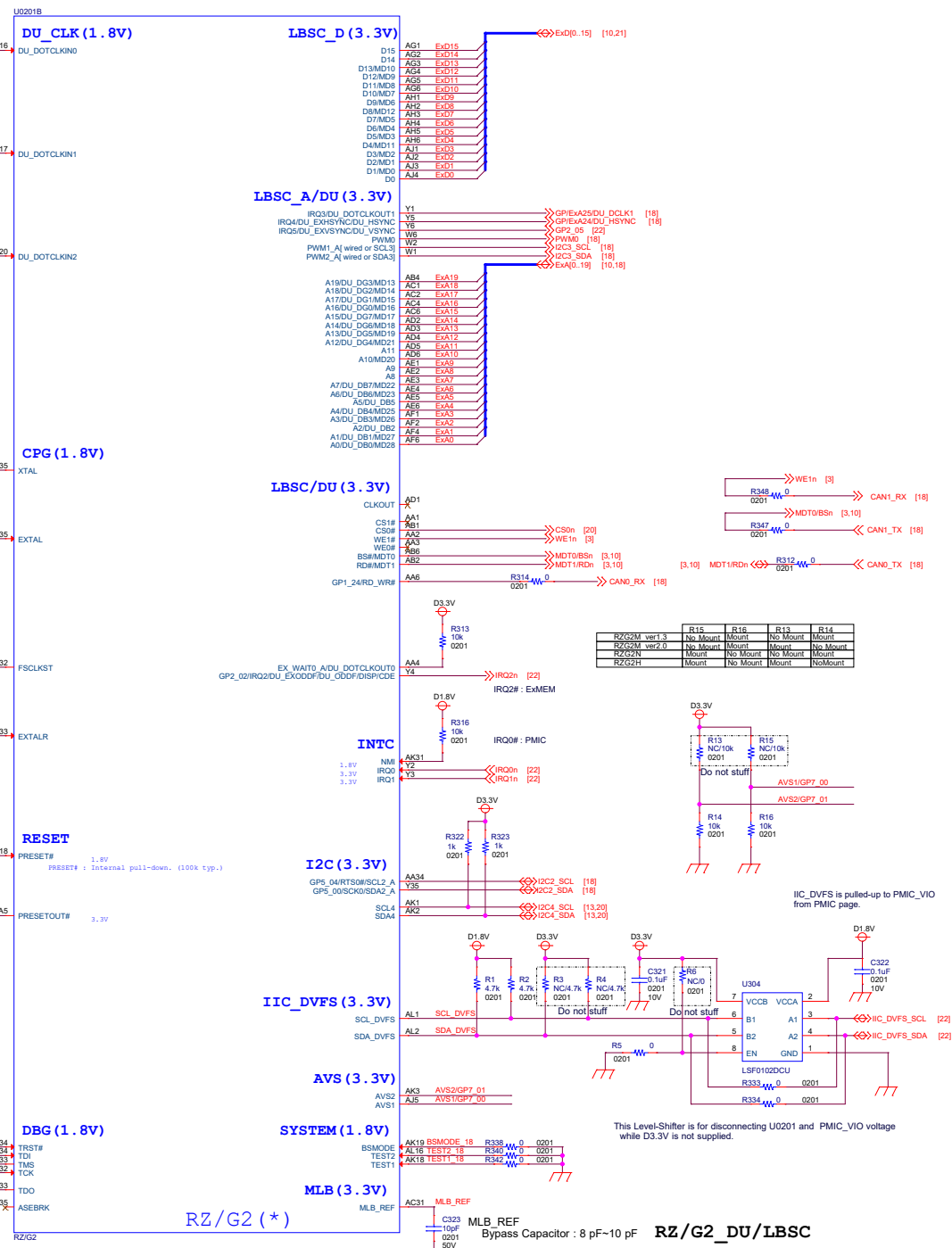
VersaLock5 have Internal Pull-down Resistor(100k-300k)

CLKINB
SEL1/SDA
SEL0/SCL
OUT0_SEL_I2CB --> 0 = Use I2C (Default)
OUT0_SEL_I2CB --> 1 = XIN/REF, XOUT (Default)
CLKSEL --> 0 = CLKIN, CLKINB
SD/OE --> = OE and active low



Be careful !!
See Pin Assignment.

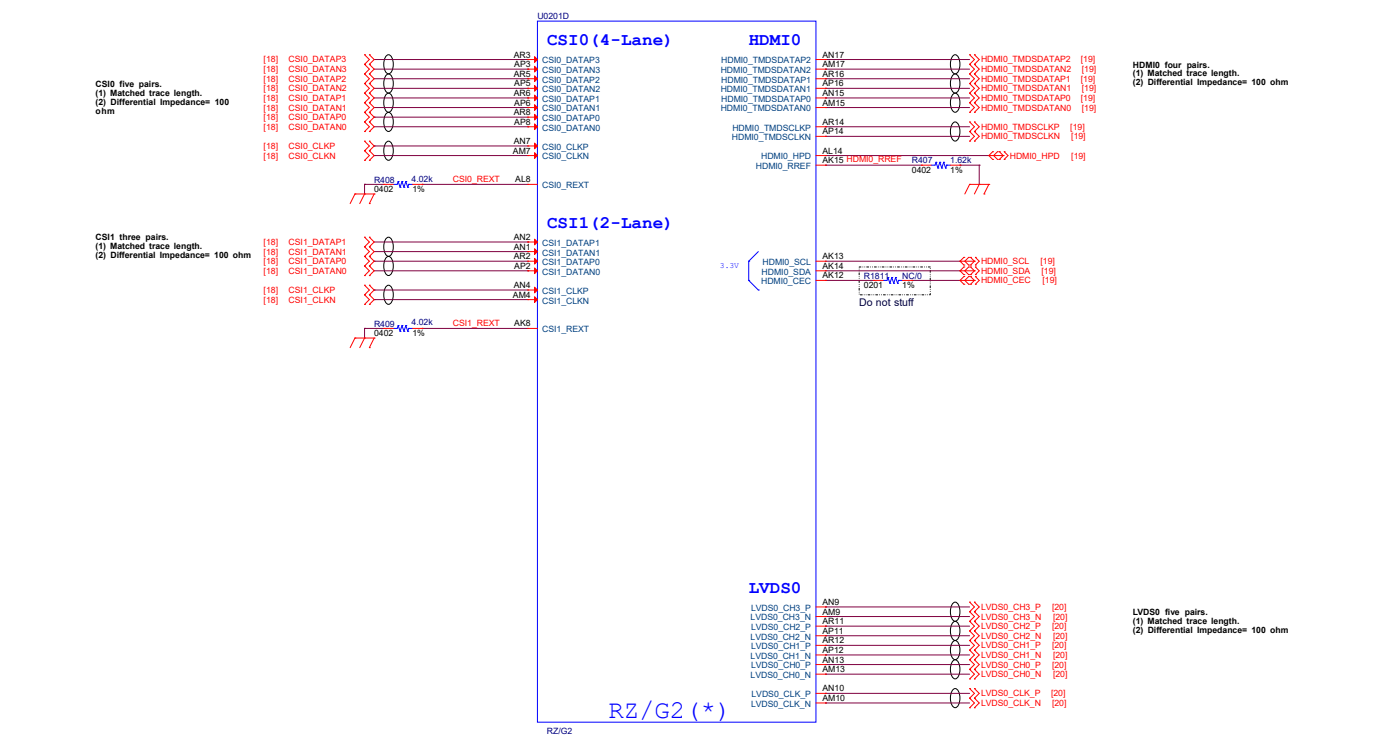
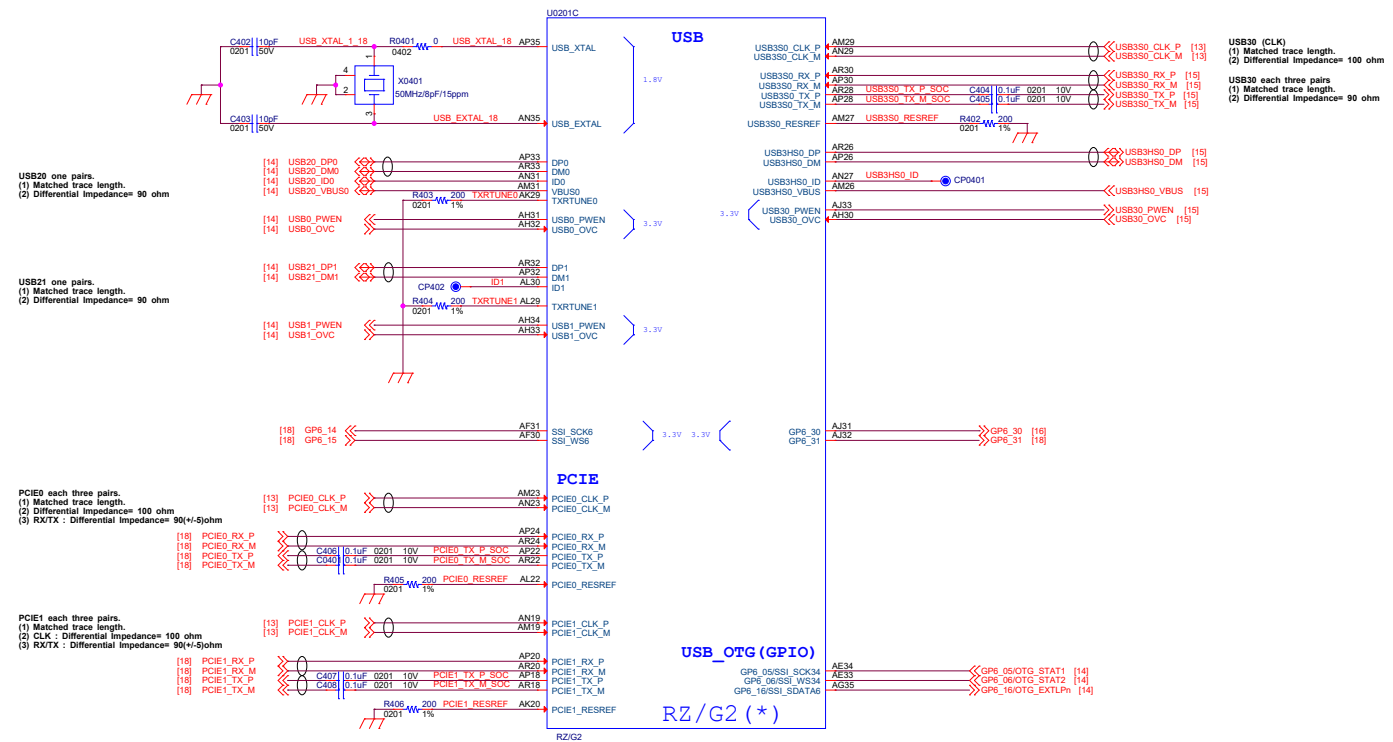
FTSH-105-01-F-D-K
[ARM_10pin]



	R16	R16	R16	R14
RZ/G2M ver1.3	No Mount	Mount	Mount	No Mount
RZ/G2M ver2.0	Mount	No Mount	No Mount	Mount
RZ/G2H	Mount	No Mount	Mount	No Mount

IIC_DVFS is pulled-up to PMIC_VIO from PMIC page.

This Level-Shifter is for disconnecting U0201 and PMIC_VIO voltage while D3.3V is not supplied.



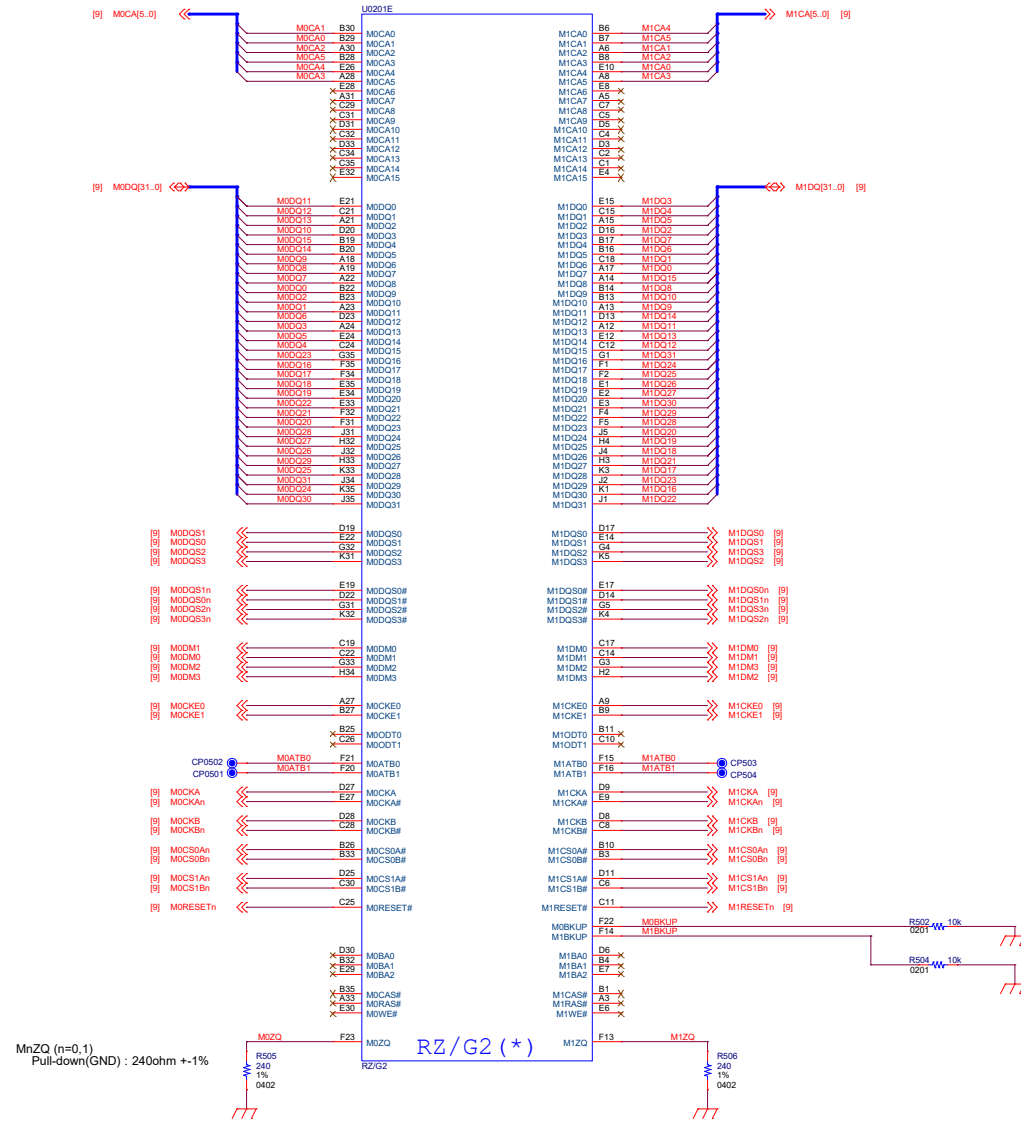
TXRTUNE_n (n=0,1)
Pull-down(GND) : 200ohm +1% 100ppm/deg

USB3Sn_RESREF (n=0)
Pull-down(GND) : 200ohm +1% 100ppm/deg

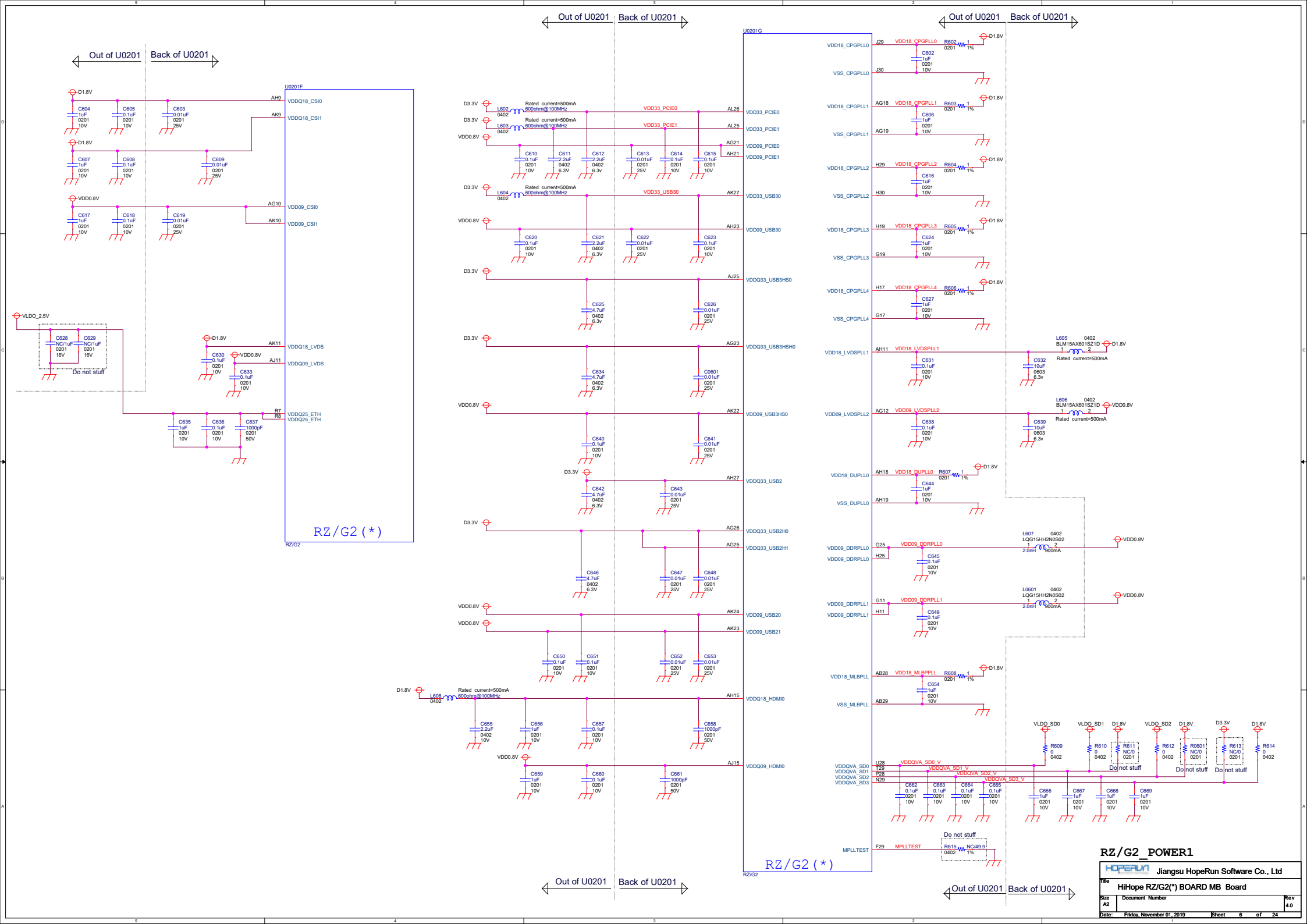
PCIEn_RESREF (n=0,1)
Pull-down(GND) : 200ohm +1% 100ppm/deg

CSIn_REXT (n=0,1)
Pull-down(GND) : 4.02kohm

HDMI_nRREF (n=0)
Pull-down(GND) : 1620ohm +1%



RZ/G2 LPDDR

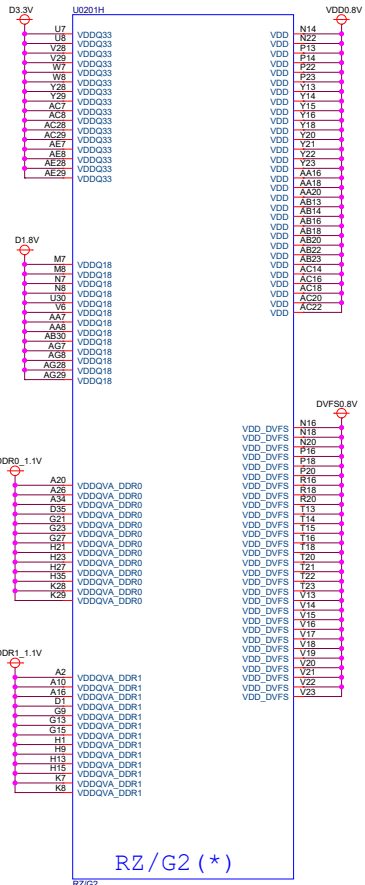


RZ/G2 (*)

RZ/G2 (*)

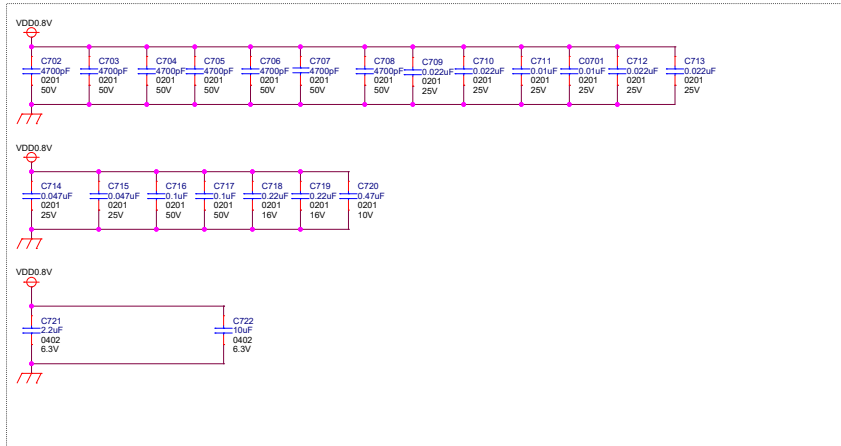
RZ/G2_POWER1

HOPE RUN		Jiangsu HopeRun Software Co., Ltd	
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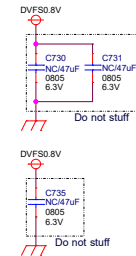
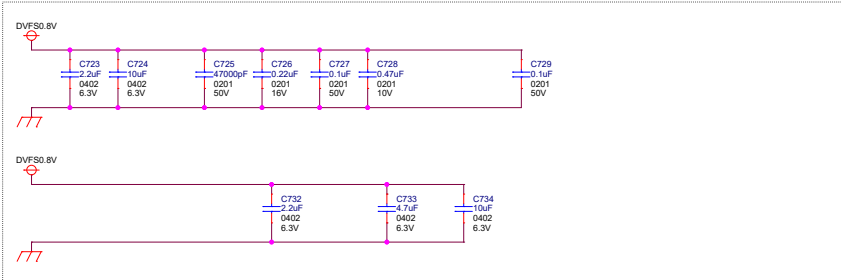


RZ/G2 (*)

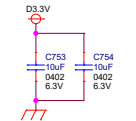
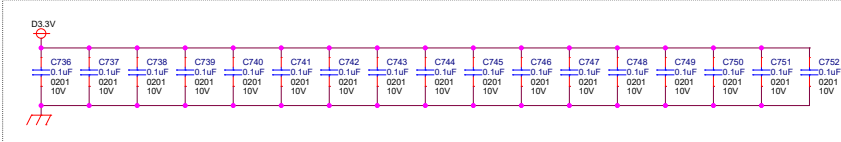
[VDD]
Back of U0201
=19pcs



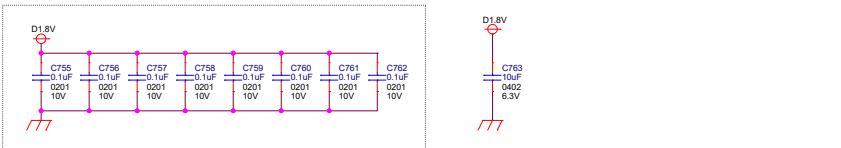
[VDD DVFS]
Back of U0201
=10pcs



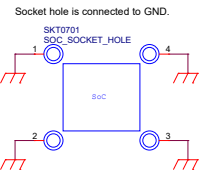
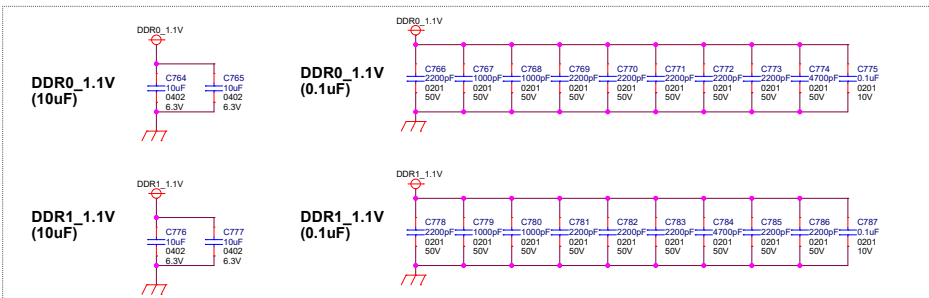
[VDDQ33]
Back of U0201
=17pcs



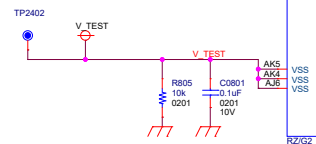
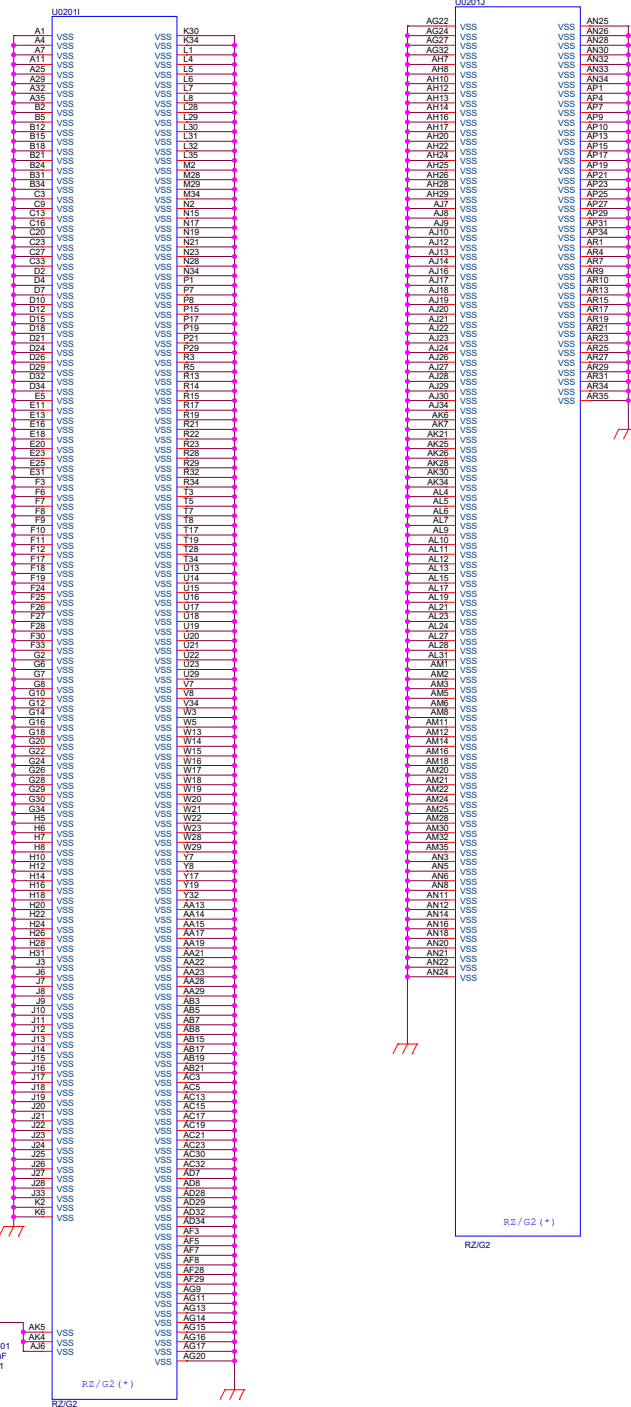
[VDDQ18]
Back of U0201
=8pcs



[DDR0/DDR1]

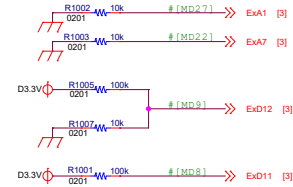
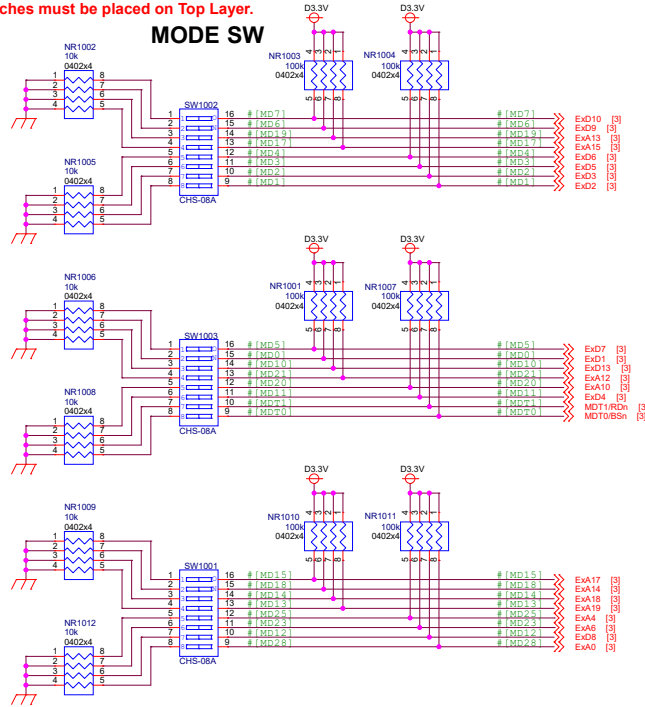


RZ/G2_POWER2

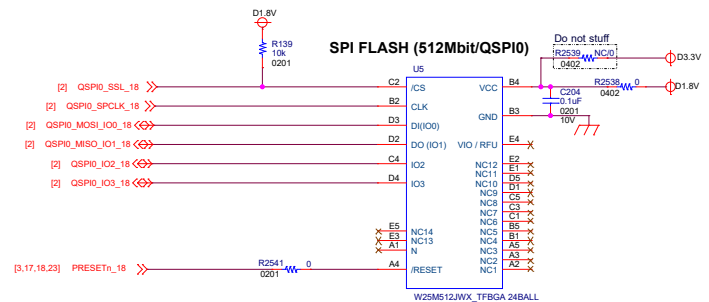


Layout Note:
Mode switches must be placed on Top Layer.

MODE SW

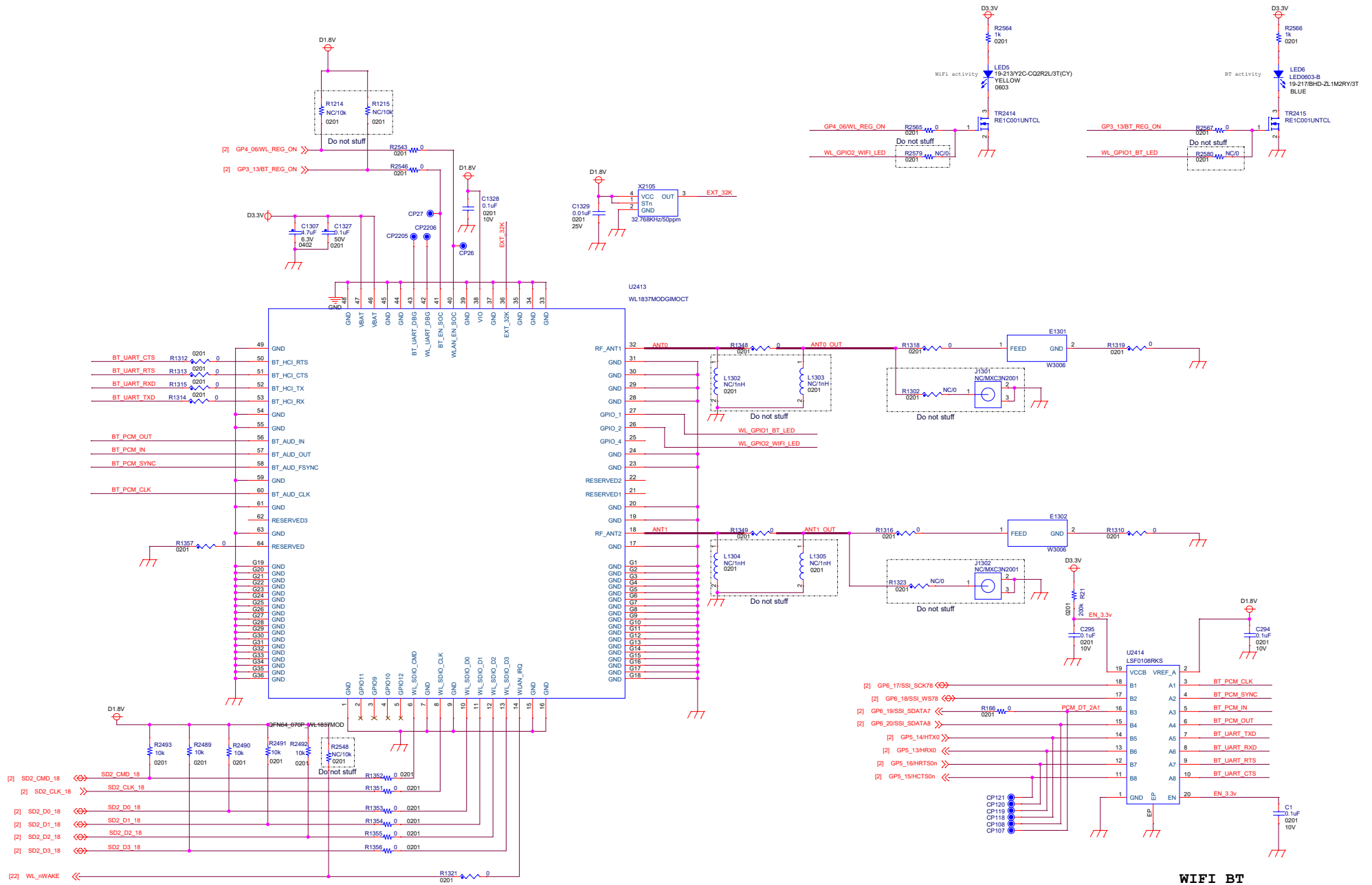


MODE SW



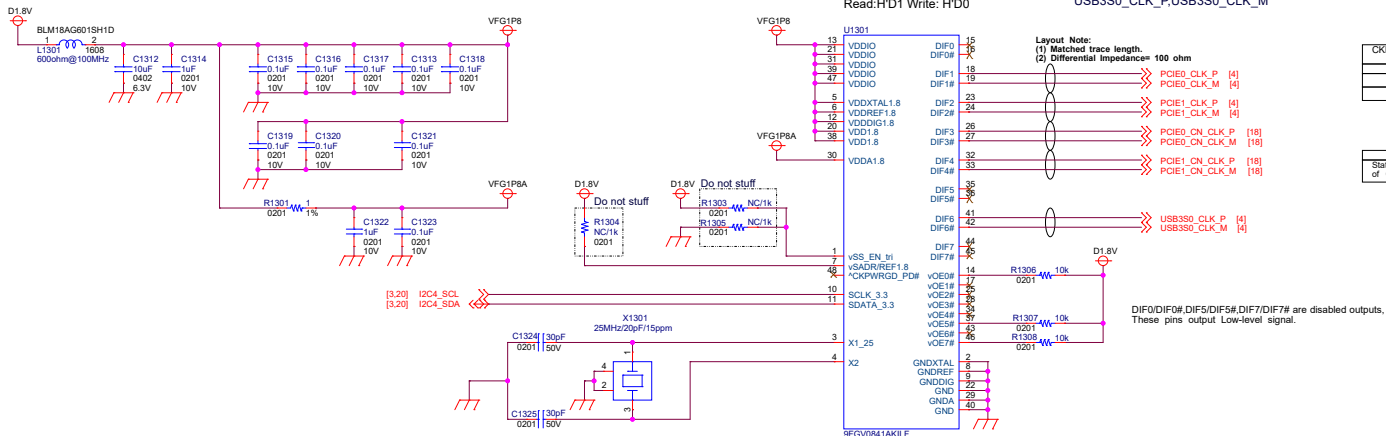
QSPI_FLASH

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WiFi_BT

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Layout Note:
Following signals need Ground guard.

PCIE0_CLK_P, PCIE0_CLK_M, PCIE1_CLK_P, PCIE1_CLK_M
 PCIE0_CN_CLK_P, PCIE0_CN_CLK_M, PCIE1_CN_CLK_P, PCIE1_CN_CLK_M
 USB3S0_CLK_P, USB3S0_CLK_M

I2C slave address: 1101_000X
 Read: HD1 Write: HD0

Layout Note:
 (1) Matched trace length.
 (2) Differential Impedance= 100 ohm

Power Management Table

CKPWRGD_PD#	SMBus CE Bit	CE#	DIF's	True CP	Comp. CP	REF
0	X	X	Low	Low	Low	Hz-Z
1	1	0	Running	Running	Running	Running
1	0	1	Low	Low	Low	Low

SMBus Address Selection Table (I2C Slave address)

State of SADR on first application of CKPWRGD_PD#	SADR	Address	* Read/Write Bit
0	1101000	1101000	X
1	1101010	1101010	X

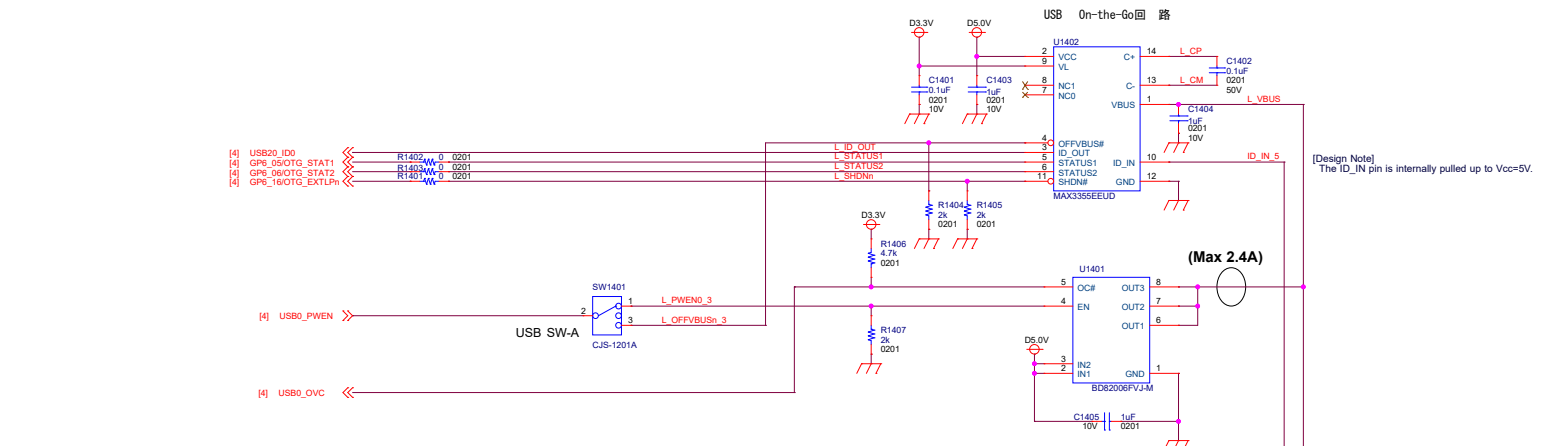
Select Spread Spectrum Table

vSS_EN_tri	Spread Spectrum
0	Spread Off
1	-0.5%

*M is Mid Voltage = 0.5VDD = 0.9V.
 This setting can be controlled by software.
 Refer to datasheet chapter of "SMBus Table : SS Readback and Control Register"

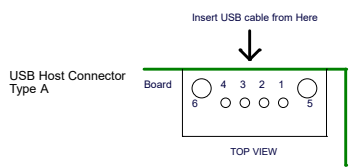
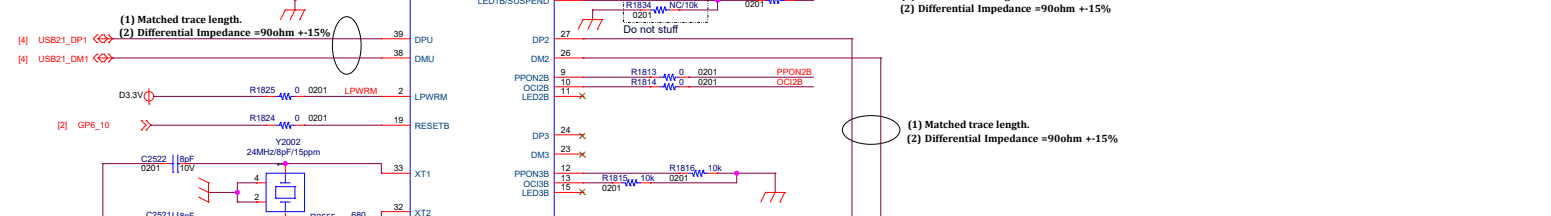
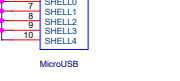
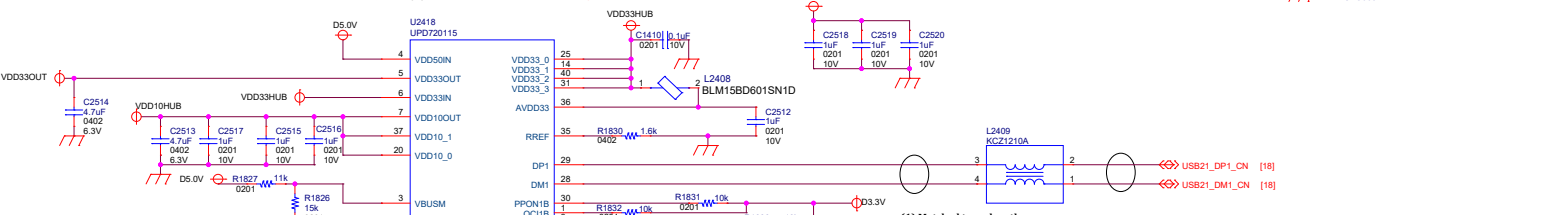
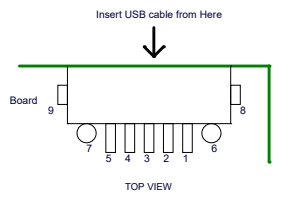
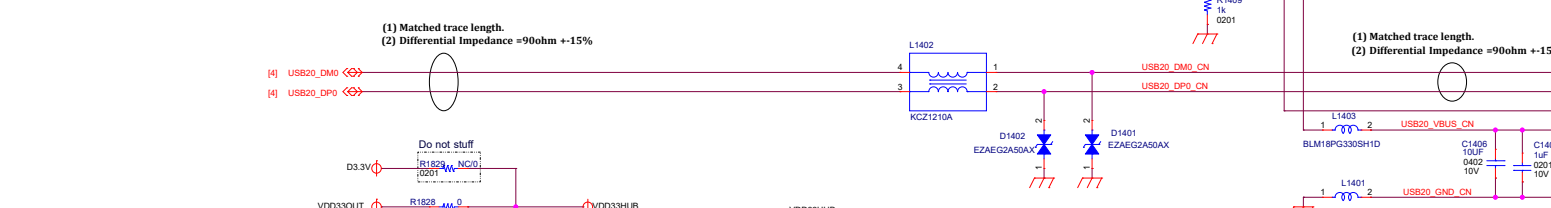
DIF0/DIF0#, DIF5/DIF5#, DIF7/DIF7# are disabled outputs.
 These pins output Low-level signal.

v : prefix indicates internal 120KOhm pull down resistor
 ^ : prefix indicates internal 120KOhm pull up resistor

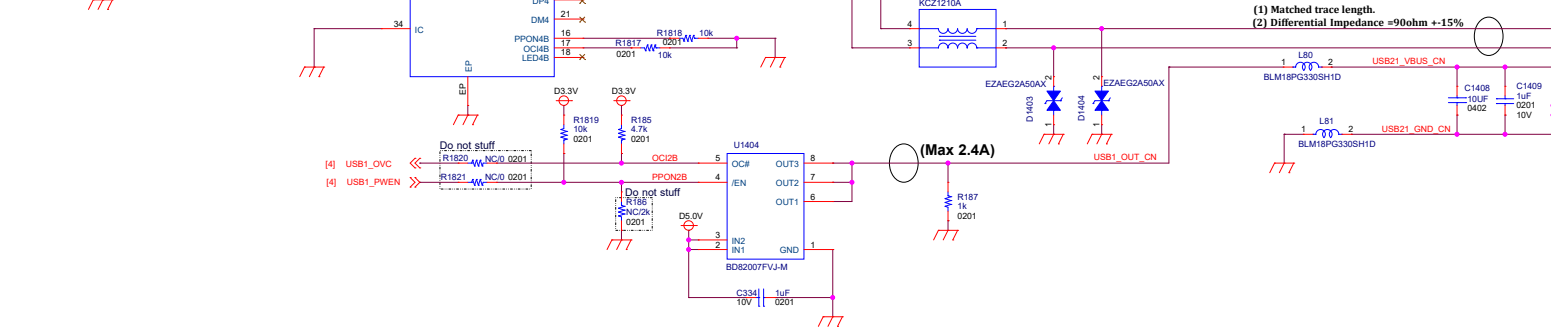


[Design Note]
The ID pin is internally pulled up to Vcc=5V.

USB2.0 ch0

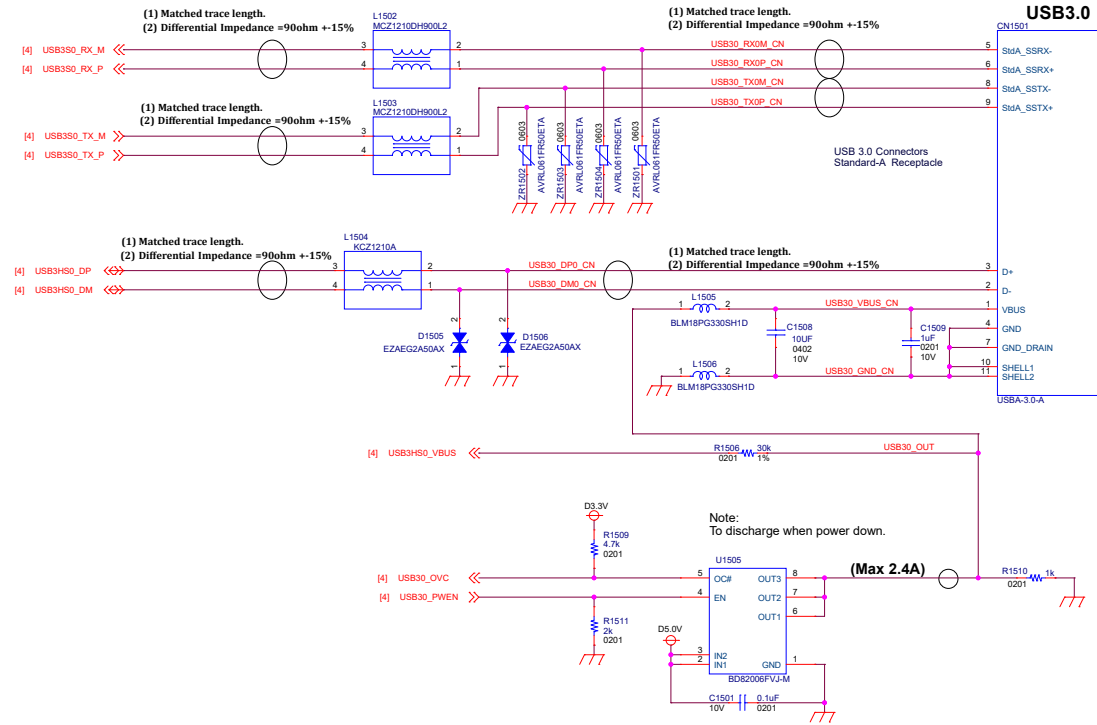


USB2.0 ch1



USB2.0

Host/Function



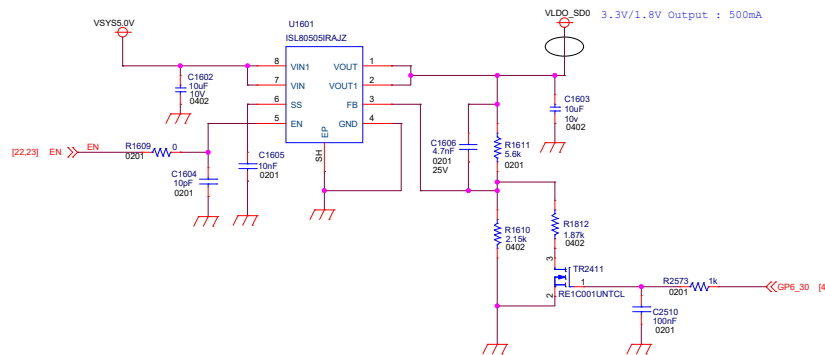
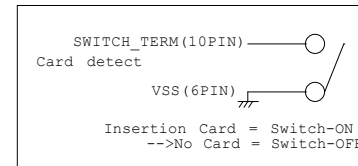
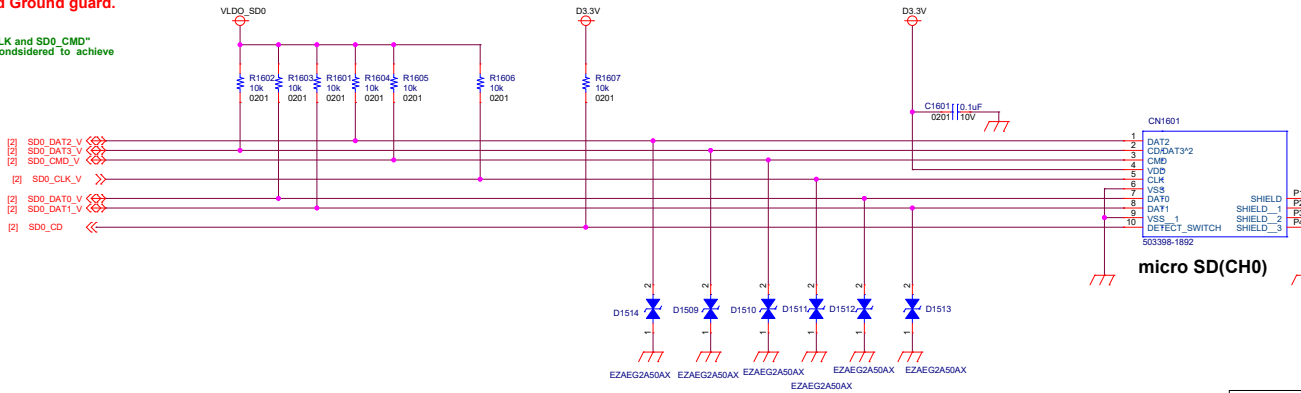
USB3.0

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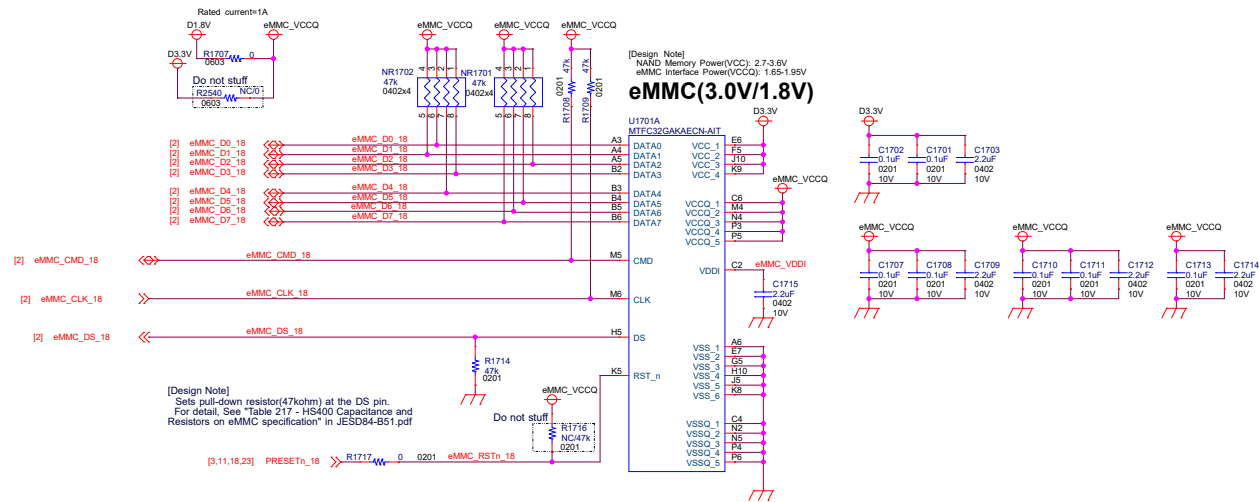
Layout Note:
Following signals need Ground guard.

SD0_CLK_V

Note: On "SD0_DAT0-3, SD0_CLK and SD0_CMD"
Dumping resistor could be considered to achieve better signal quality.



micro SD card



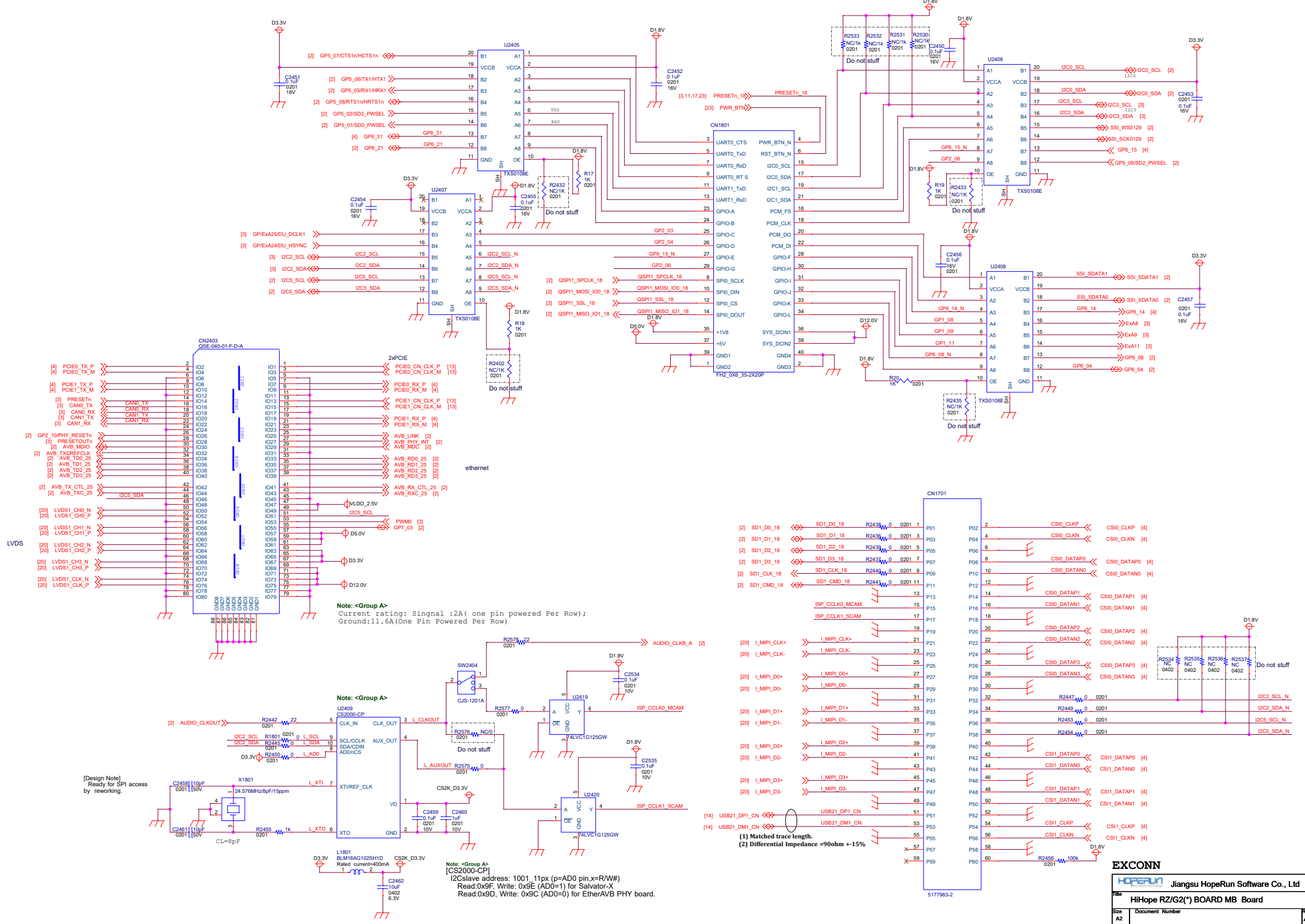
Layout Note:
Make line impedance of SDx_XXX and eMMC_XXX_18 to be less than 75ohm.

Layout Note:
Following signals need Ground guard.
SD2_CLK/NFDATA8_V, eMMC_CLK_18,

Layout Note:
Matched Trace Length from RZ/G2M to eMMC. max 400Mbps/pin

Group 1
eMMC_D[7:0]_18
eMMC_CMD_18
eMMC_CLK_18
eMMC_DS_18

U1701B		MTFC32GAKAECN-AIT	
A1	NC_1	NC_67	K1
A2	NC_2	NC_68	K2
A3	NC_3	NC_69	K3
A4	NC_4	NC_70	K4
A5	NC_5	NC_71	K5
A6	NC_6	NC_72	K6
A7	NC_7	NC_73	K7
A8	NC_8	NC_74	K8
A9	NC_9	NC_75	K9
B1	NC_10	NC_76	K10
B2	NC_11	NC_77	K11
B3	NC_12	NC_78	K12
B4	NC_13	NC_79	M1
B5	NC_14	NC_80	M2
B6	NC_15	NC_81	M3
B7	NC_16	NC_82	M4
B8	NC_17	NC_83	M5
B9	NC_18	NC_84	M6
C1	NC_19	NC_85	M11
C2	NC_20	NC_86	M12
C3	NC_21	NC_87	M13
C4	NC_22	NC_88	M14
C5	NC_23	NC_89	M15
C6	NC_24	NC_90	N1
C7	NC_25	NC_91	N2
C8	NC_26	NC_92	N3
C9	NC_27	NC_93	N4
C10	NC_28	NC_94	N5
C11	NC_29	NC_95	N6
C12	NC_30	NC_96	N7
C13	NC_31	NC_97	N8
C14	NC_32	NC_98	N9
C15	NC_33	NC_99	N10
C16	NC_34	NC_100	N11
D1	NC_35	NC_101	P1
D2	NC_36	NC_102	P2
D3	NC_37	NC_103	P3
D4	NC_38	NC_104	P4
D5	NC_39	NC_105	P5
D6	NC_40	NC_106	P6
D7	NC_41	NC_107	P7
D8	NC_42	NC_108	P8
D9	NC_43	NC_109	P9
E1	NC_44	NC_45	
E2	NC_46	NC_47	
E3	NC_48	RFU_1	A7
E4	NC_49	RFU_2	A8
E5	NC_50	RFU_3	A9
E6	NC_51	RFU_4	A10
E7	NC_52	RFU_5	A11
E8	NC_53	RFU_6	A12
E9	NC_54	RFU_7	A13
F1	NC_55	RFU_8	A14
F2	NC_56	RFU_9	A15
F3	NC_57	RFU_10	A16
F4	NC_58	RFU_11	A17
F5	NC_59		
F6	NC_60		
J1	NC_61		
J2	NC_62		
J3	NC_63		
J4	NC_64		
J5	NC_65		
J6	NC_66		



Note: <Group A>
 Current rating: Signal: 2A (one pin powered Per Row);
 Ground: 1.6A (One Pin Powered Per Row)

Note: <Group A>
 CS[2000-CP]

Note: <Group A>
 [CS2000-CP]
 I2C slave address: 1001 11px (p=AD0 pin,x=R/W#)
 Read: 0x9F, Write: 0x9E (AD0=1) for Salvator-X
 Read: 0x9D, Write: 0x9C (AD0=0) for EtherAVB PHY board.

[Design Note]
 Ready for SPI access
 by reworking.

- [2] I_MPL_CLK+
- [2] I_MPL_CLK-
- [2] I_MPL_D0+
- [2] I_MPL_D0-
- [2] I_MPL_D1+
- [2] I_MPL_D1-
- [2] I_MPL_D2+
- [2] I_MPL_D2-
- [2] I_MPL_D3+
- [2] I_MPL_D3-

- [14] USB21_DP1_CN
- [14] USB21_DM1_CN

(1) Matched trace length.
 (2) Differential Impedance = 90ohm ± 15%

EXCONN
 HiHope RZ/G2(*) BOARD MB Board

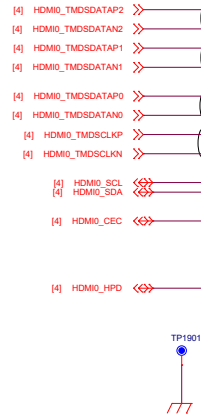
HiHope
 Jianguo HopeRun Software Co., Ltd

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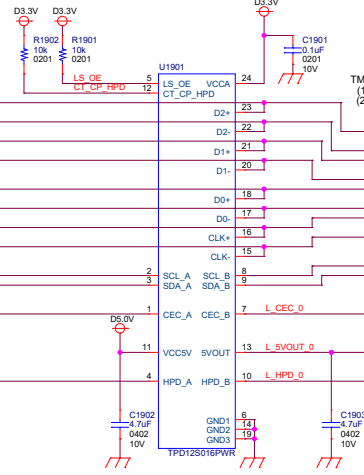
Layout Note:

Matched trace length from SoC until CN1901
 HDMI0_TMDSDATAP2, HDMI0_TMDSDATAN2
 HDMI0_TMDSDATAP1, HDMI0_TMDSDATAN1
 HDMI0_TMDSDATAP0, HDMI0_TMDSDATAN0
 HDMI0_TMDSCLKP, HDMI0_TMDSCLKN

TMDS four pairs.
 (1) Matched trace length.
 (2) Differential Impedance= 100 ohm

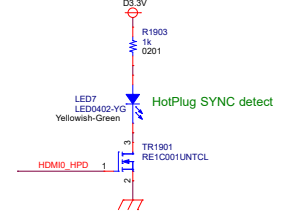
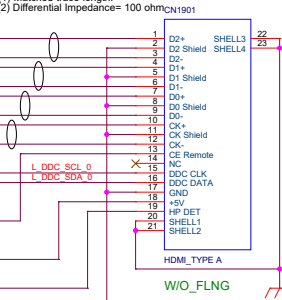


**HDMI COMPANION CHIP
 WITH ESD PROTECTION, I2C LEVEL SHIFTER**



HDMI output(HDMI0)

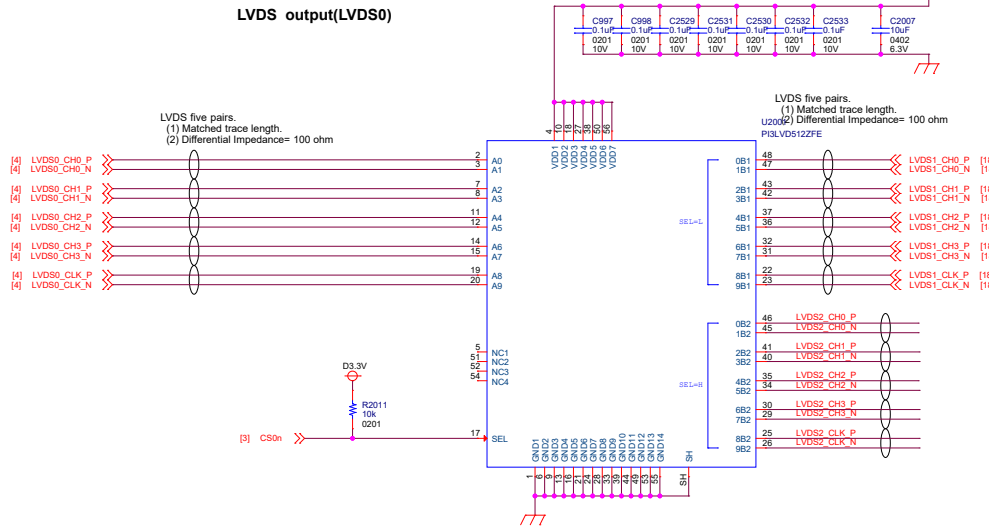
TMDS four pairs.
 (1) Matched trace length.
 (2) Differential Impedance= 100 ohm



HDMI_OUT

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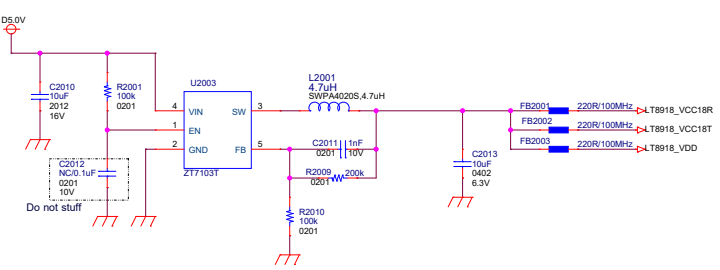
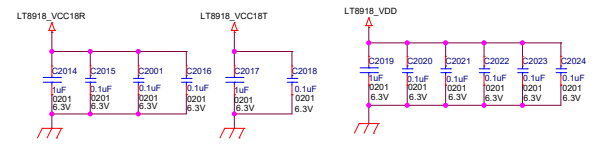
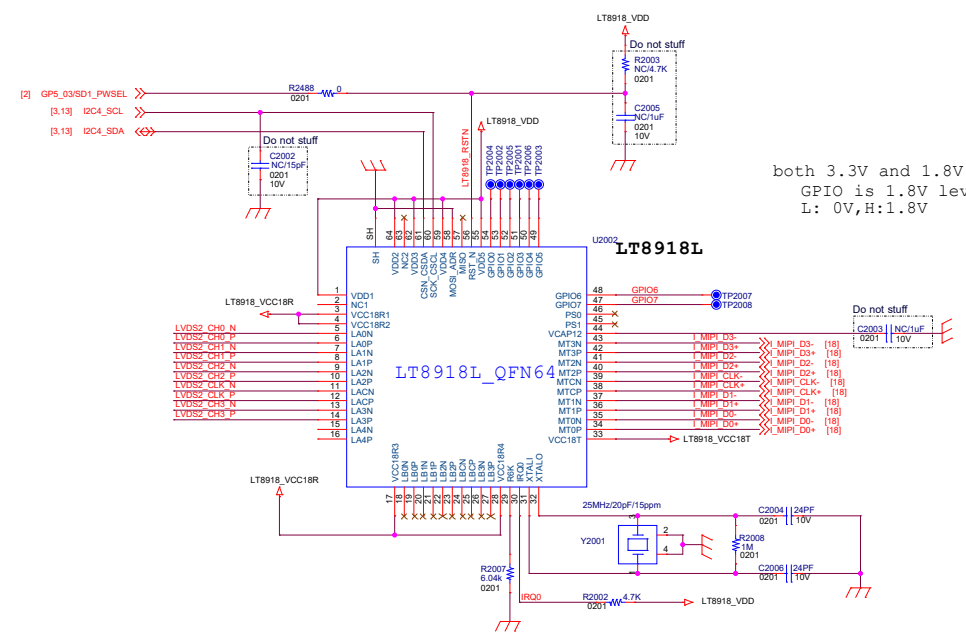
LVDS output(LVDS0)



LVDS five pairs.
(1) Matched trace length.
(2) Differential Impedance= 100 ohm

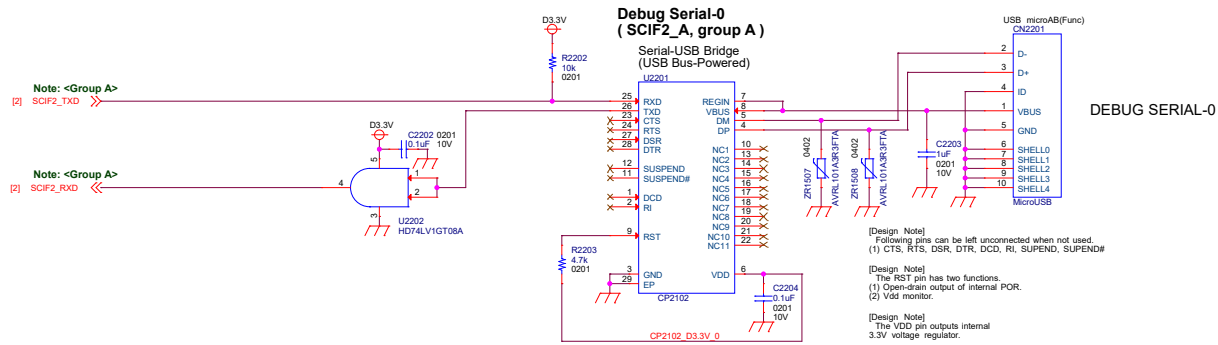
LVDS five pairs.
(1) Matched trace length.
(2) Differential Impedance= 100 ohm

both 3.3V and 1.8V is OK.
GPIO is 1.8V level:
L: 0V,H:1.8V



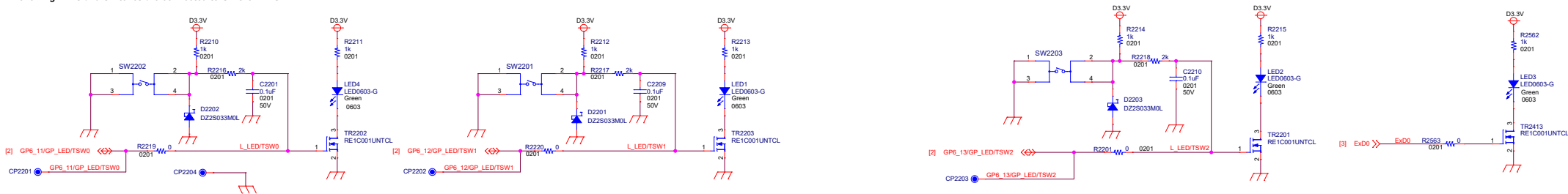
LVDS0 TO MIPI

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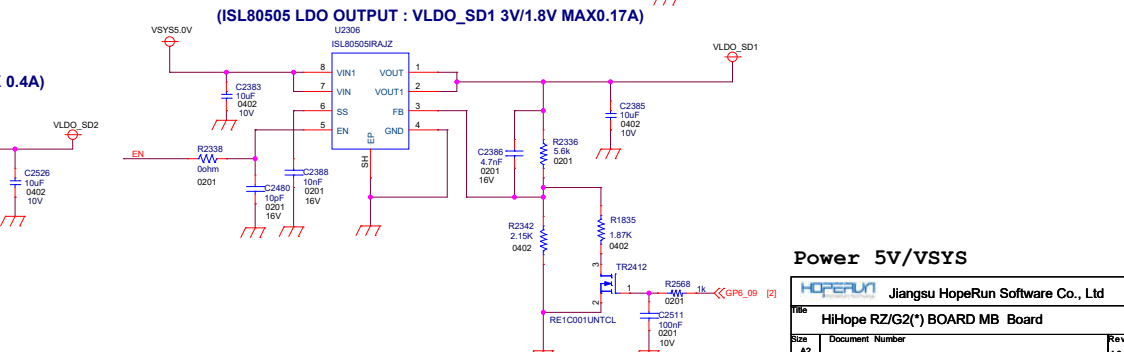
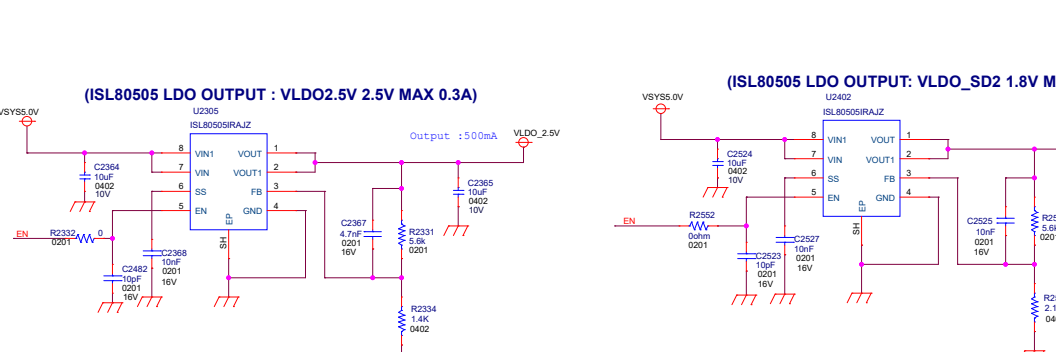
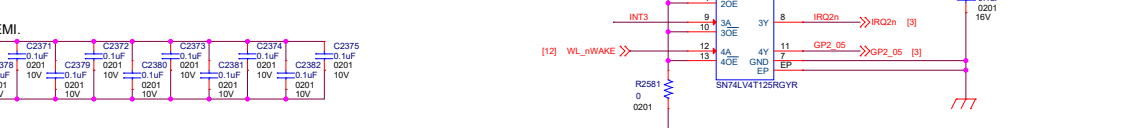
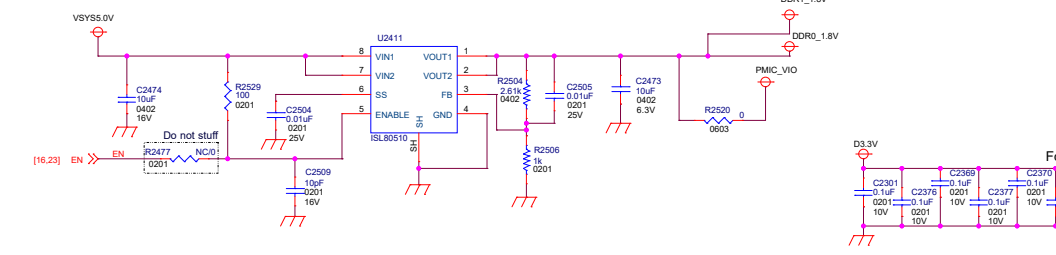
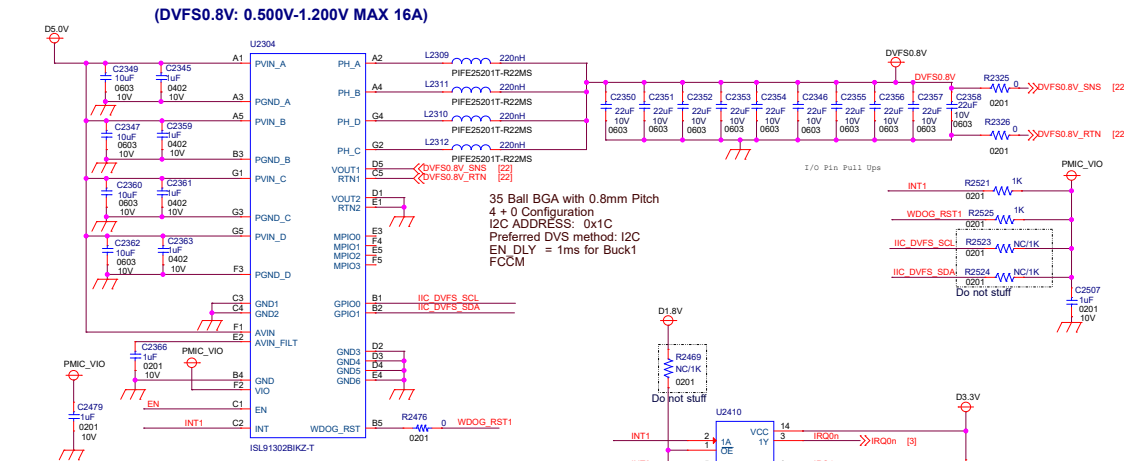
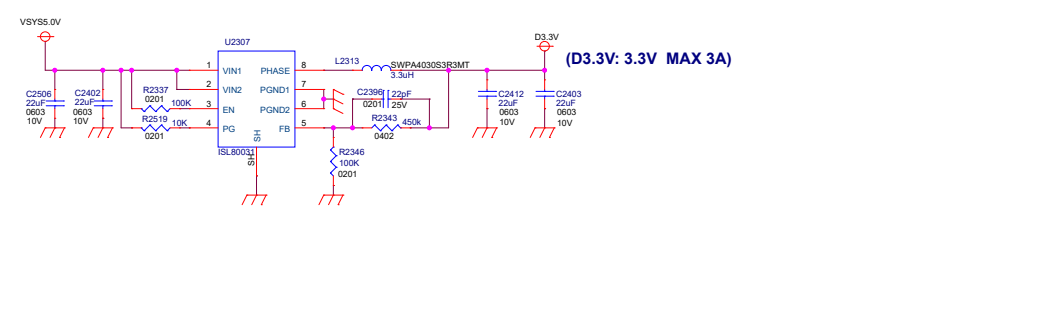
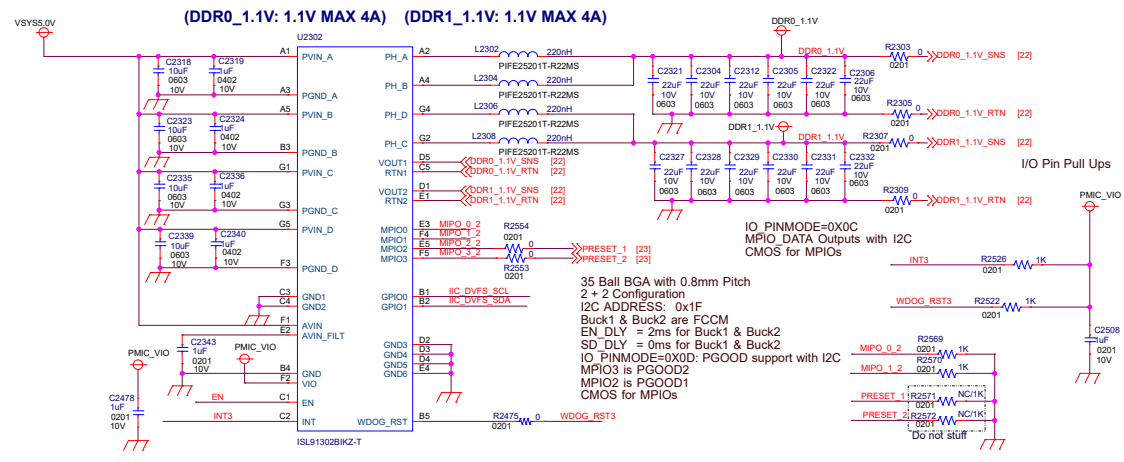
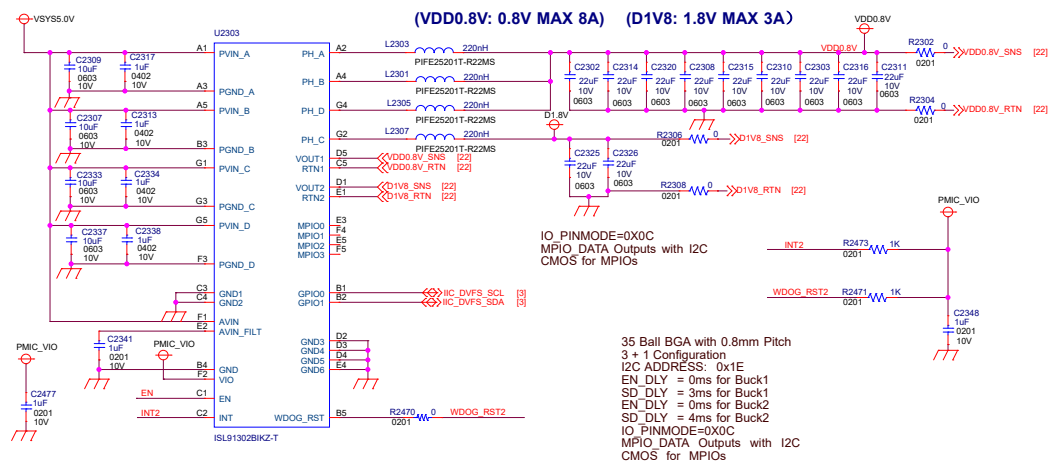
GPLED / Tact Switch

General Purpose LEDs or Tactile Switches connected to GPIO of RZ/G2M

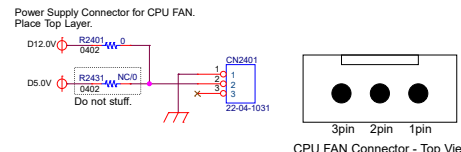
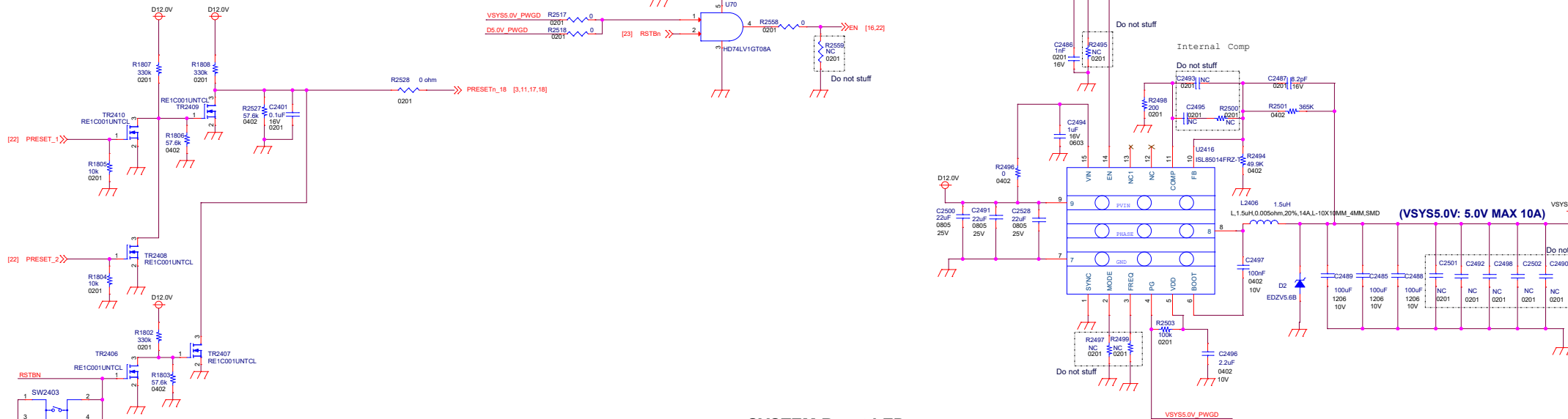
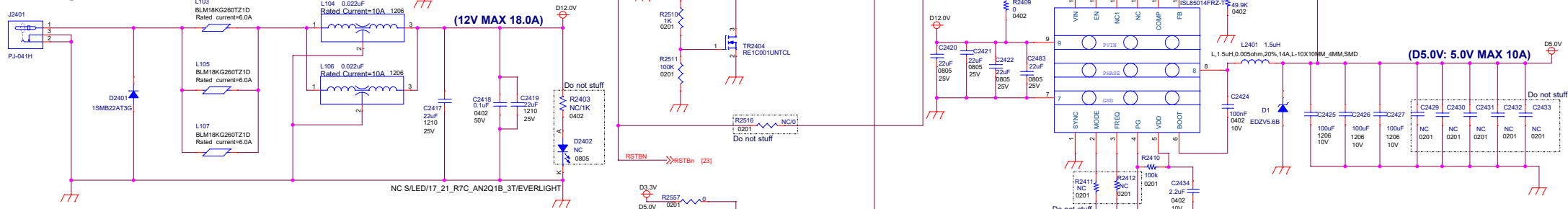


DEBUG_SCIF/LED/TactSW

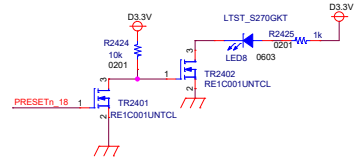
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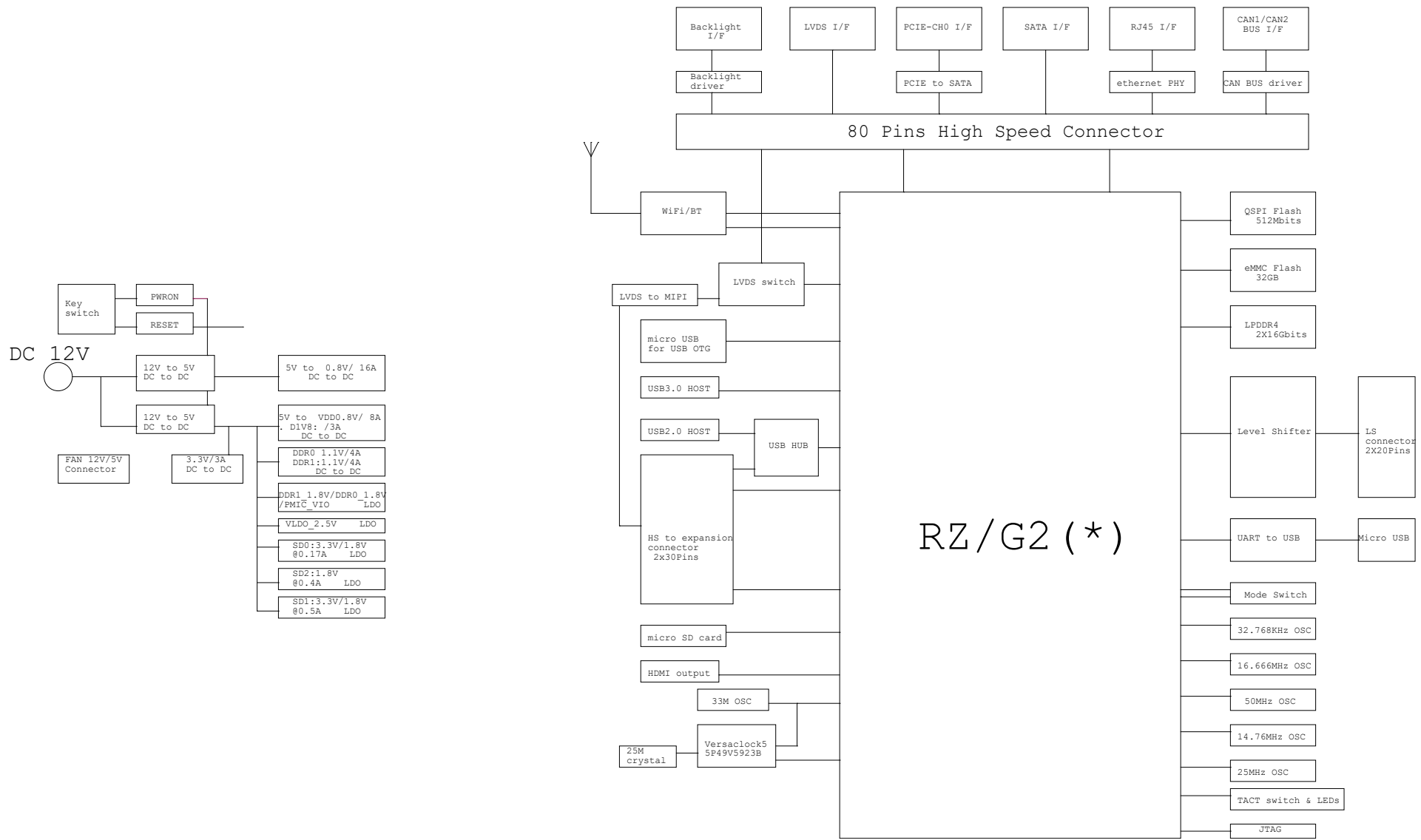
DC12V Input



SYSTEM Reset LED



Power PMIC



BLOCK DIAGRAM

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